WHAT IS CLAIMED IS:

1. A read/write memory device, comprising:

a clock switching means for switching between a first clock signal and a second clock signal;

a single-port random access memory (RAM) module for storing data; and

a random access memory (RAM) clock for synchronizing the clock signals with the random access memory (RAM) module.

2. The read/write memory device of claim 1, further comprising:

means to accept signals from a first host and a second host, the signals including the first clock signal and the second clock signal.

3. The read/write memory device of claim 2, wherein the means to accept signals further comprises a first host and a second host, the first host having a first clock and the second host having a second clock, the signals including the first clock signal and the second clock signal.

4. The read/write memory device of claim 2, further comprising:

an address and data bus component.

5. The read/write memory device of claim 2, further comprising:

a control signal selection component for controlling the selection of the signals from the first host and the second host to the random access memory (RAM) module.

6. The read/write memory device of claim 2, wherein:

the clock switching means further comprises a clock switching unit with a first local clock gating cell to control the first clock signal and a control signal from the first host, and a second local clock gating cell for controlling the second clock signal and a control signal from the second host.

7. The read/write memory device of claim 6, further comprising:

a random access memory (RAM) clock for accepting the signals from the first local clock gating cell and the second local clock gating cell.

8. The read/write memory device of claim 7, wherein:

the output of the RAM clock is fed into the single-port random access memory (RAM) module for storing data.

9. A read/write memory system, comprising:

a first host and a second host, the first host having a first clock generating a first clock signal and the second host having a second clock generating a second clock signal;

a clock switch for switching between the first clock signal and the second clock signal;

a single-port random access memory (RAM) module for storing data; and

a RAM clock for synchronizing the clock signals with the random access memory (RAM) module.

10. The read/write memory device of claim 9, further comprising:

a control signal selection component for controlling the selection of the signals from the first host and the second host to the random access memory (RAM) module.

11. The read/write memory device of claim 9, wherein:

the clock switching means further comprises a clock switching unit with a first local clock gating cell to control the first clock signal and a control signal from the first host, and a second local clock gating cell for controlling the second clock signal and a control signal from the second host.

12. A method for storing and recalling data in a memory device, comprising the steps of:

generating a first clock signal and a second clock signal;

switching between the first clock signal and the second clock signal;

allowing either the first clock signal or the second clock signal access to a single-port random access memory (RAM) module; and

storing and recalling the stored data from the random access memory (RAM) module.

13. The method of claim 12, further comprising the step of:

providing a first host and second host, wherein the first host includes a first clock that generates the first clock signal, and the second host includes a second clock generating the second clock signal.

14. The method of claim 12, further comprising the step of:

controlling the selection of the signals from the first host and the second host to the random access memory (RAM) module.

15. The method of claim 14, further comprising the steps of:

controlling the first clock signal and a control signal from the first host; and

controlling the second clock signal and a control signal from the second host.

16. The method of claim 15, wherein the first clock signal and the second clock signal are input to a random access memory (RAM) clock.

17. The method of claim 16, further comprising the step of:

feeding the output of the random access memory (RAM) clock into the single port random access memory (RAM) module.

18. A method for storing and recalling data in a memory device, comprising the steps of:

switching between a first clock signal and a second clock signal;

storing data in a single port random access memory (RAM) module; and

synchronizing the clock signals with the random access memory (RAM) module.

19. The method of claim 18, further comprising the step of:

providing a first host and second host, wherein the first host includes a first clock that generates the first clock signal, and the second host includes a second clock generating the second clock signal.

20. The method of claim 18, further comprising the step of:

controlling the selection of the signals from the first host and the second host to the random access memory (RAM) module.

21. The method of claim 20, further comprising the steps of:

controlling the first clock signal and a control signal from the first host; and

controlling the second clock signal and a control signal from the second host.